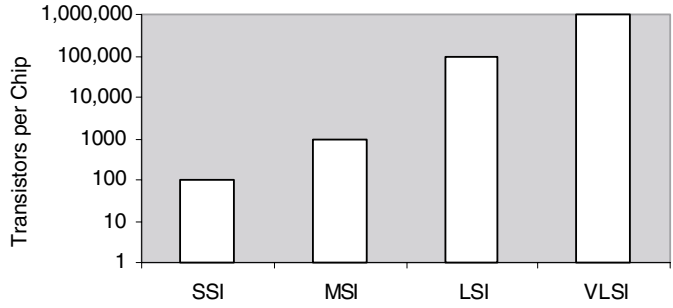

FIGURE 2.7 Relative component count of ICs.

As IC densities grew at this tremendous pace, the number of pins on each IC and the speed at which they operated began to increase as well. DIPs soon become a limiting factor in the performance of ICs. First, the addition of more pins made the package longer, because there are only two rows of pins. However, most chips are relatively square in shape to minimize on-chip interconnection distances. This creates a conflict: a long, narrow package that is unsuitable for increasing square die sizes. Second, the lengths of some pins in the DIP lead frame, especially those near the corners, are relatively long. This has an adverse impact on the quality of high-speed signals. Third, the 0.1-in pin spacing on DIPs keeps them artificially large as circuit board technologies continue improving to handle smaller contacts.

One solution to the pin density problem was the development of the *pin grid array*, or PGA, package. Shown in Fig. 2.8, the PGA is akin to a two-dimensional DIP with pins spaced on 0.1-in centers. Very high pin counts are achievable with a PGA, because all of its area is usable rather than just the perimeter. Being a square, the PGA is compatible with large ICs, because it more closely matches the proportions of a silicon chip.

The PGA provides high pin density, but its drawback is relatively high cost. Two lower-cost packages were developed for ICs that require more pins than DIPs but fewer pins than found on a PGA: the *small outline integrated circuit* (SOIC) and the *plastic leaded chip carrier* (PLCC). Examples of SOIC and PLCC packages are shown in Fig. 2.9. Both SOICs and PLCCs feature pins on a 0.05-in pitch — half that of a DIP or PGA. The SOIC is basically a shrunken DIP with shorter pins that are folded parallel to the plane of the package instead of protruding down vertically. This enables the SOIC to be surface mounted onto the circuit board by soldering the pins directly to metal pads on the board. By contrast, a DIP requires that holes be drilled in the board for the pins to be soldered into. The SOIC represents an improvement in packaging density and ease of manufacture over DIPs, but it is still limited to relatively simple ICs due to its one-dimensional pin arrangement.

PLCCs increase pin density and ease the design of the lead frame by utilizing a two-dimensional pin arrangement. Higher pin counts (68, 84, and 96 pins) were enabled by the PLCC, and its square

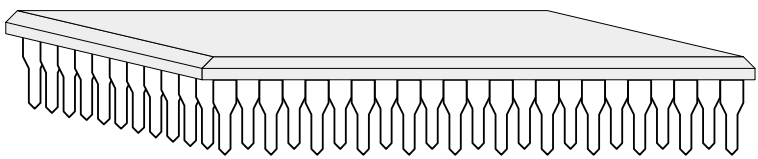

FIGURE 2.8 Pin grid array package.

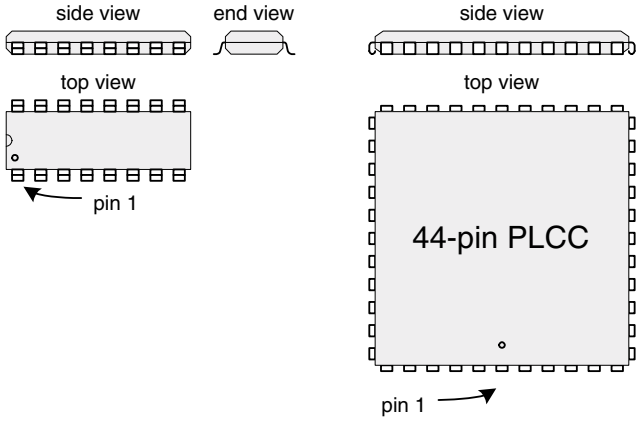

FIGURE 2.9 SOIC and PLCC.

design is more capable of accepting larger silicon dice than either the DIP or SOIC. PLCC leads are not bent outward, as in the case of a SOIC, but are curved inward in a "J" pattern. The more similar aspect ratio of the PLCC package and the dice that are placed into them enabled lead frames with shorter and more consistent pin lengths, reducing the degrading effects on high-speed signals.

A higher-density relative of the PLCC and SOIC is the *quad flat pack*, or QFP. A QFP resembles a PLCC in terms of its square or rectangular shape but has leads that are bent outward like an SOIC. Additionally, QFP leads are thinner and spaced at a smaller pitch to achieve more than twice the lead density of a comparably sized PLCC.

Perhaps the most widely used package for high-density ICs is the *ball grid array*, or BGA. The BGA is a surface mount analog to the PGA with significantly higher ball density. Contact is made between a BGA and a circuit board by means of many small preformed solder balls that adhere to contacts on the bottom surface of the BGA package. Figure 2.10 illustrates the general BGA form factor, but numerous variants on aspect ratio and ball pitch exist. Typical ball pitch ranges from 1.27 mm down to 0.8 mm, and higher densities are on the way.

There are many variations of the packaging technologies already mentioned. Most packages comply with industry standard dimensions, but others are proprietary. Semiconductor manufacturers provide detailed drawings of their packages to enable the proper design of circuit boards for their products.

2.3 THE 7400-SERIES DISCRETE LOGIC FAMILY

With the advent of ICs in the early 1960s, engineers needed ready access to a library of basic logic gates so that these gates could be wired together on circuit boards and turned into useful products. Rather than having to design a custom microchip for each new project, semiconductor companies

FIGURE 2.10 Ball grid array.